



UV4407S
-30V -13A P-Channel Mosfet

General Description

The UV4407S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge.

This device is suitable for use in PWM, load switching and general purpose applications.

Features

Enhancement Mode

Enhanced Body diode dv/dt capability

100% Avalanche Tested

V_{DS}	-30	V
$R_{DS(on)\ TYP}@V_{GS}=-10V$	10	$m\Omega$
$R_{DS(on)\ TYP}@V_{GS}=-4.5V$	15	$m\Omega$
I_D	-13	A

Applications

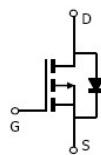
Power switching application

Hard Switched and High Frequency Circuits

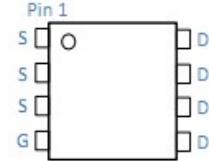
Uninterruptible Power Supply



SOP8LTOPview



Schematic diagram

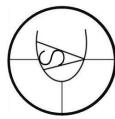


Package Marking And Ordering Information

Part ID	Package Type	Marking	Tape and Reel information
UV4407S	SOP8L	UV4407S	3000pcs/Reel

Maximum ratings, at $T_j=25^\circ C$, unless otherwise specified

Symbol	Parameter	Rating	Unit
$V_{(BR)DSS}$	Drain –Source breakdown voltage	-30	V
I_D	Continuous drain current (Silicon Limited)	$T_c=25^\circ C$	-13
		$T_c=100^\circ C$	-9
I_{DM}	Pulse drain current tested①	$T_c=25^\circ C$	-52
E_{AS}	Avalanche energy, single pulsed②	51.25	mJ
P_D	Maximum power dissipation	$T_c=25^\circ C$	3
V_{GS}	Gate-Source voltage	± 20	V
$T_{STG}\ T_J$	Storage and operating temperature range	-55 to 175	°C



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Thermal Characteristic

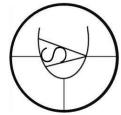
Symbol	Parameter	Typical	Unit
R_{QJC}	Thermal Resistance-Junction to Case	0.8	°C/W
R_{QJA}	Thermal Resistance-Junction to Ambient	40	°C/W

Typical Characteristics

Symbol	Parameter	Condition	Min	Type	Max	Unit
Static Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$			1	μA
	Zero Gate Voltage Drain Current($T_j=100^\circ\text{C}$)	$V_{DS}=-24\text{V}$, $V_{GS}=0\text{V}$			50	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS}=\pm 20\text{V}$, $V_{BS}=0\text{V}$			± 100	nA
$V_{GS(\text{TH})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	-1.2	-1.8	-2.8	V
$R_{DS(\text{ON})}$	Drain-Source On-State Resistance ^③	$V_{GS}=-10\text{V}$, $I_D=-13\text{A}$		10	12	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$, $I_D=-9\text{A}$		15	19.5	$\text{m}\Omega$
Dynamic Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise stated)						
C_{iss}	Input Capacitance	$V_{DS}=-15\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$		2350		PF
C_{oss}	Output Capacitance			330		PF
C_{rss}	Reverse Transfer Capacitance			139		PF
Q_g	Total Gate Charge	$V_{DS}=-15\text{V}$, $I_D=-13\text{A}$, $V_{GS}=-10\text{V}$		29.8		nC
Q_{gs}	Gate-Source Charge			4.7		nC
Q_{gd}	Gate-Drain Charge			10		nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay time	$V_{DD}=-15\text{V}$, $I_D=-12\text{A}$, $R_G=1\Omega$, $V_{GS}=-10\text{V}$		11		nS
t_r	Turn-on Rise time			9		nS
$t_{d(off)}$	Turn-off Delay time			25		nS
t_f	Turn-off Fall time			13		nS
Source-Drain Diode Characteristics						
V_{SD}	Forward on voltage	$I_{SD}=-3.5\text{A}$, $V_{GS}=0\text{V}$		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	$T_j=25^\circ\text{C}$, $I_{SD}=-13\text{A}$		39		nS
Q_{rr}	Reverse Recovery Charge			22		nC

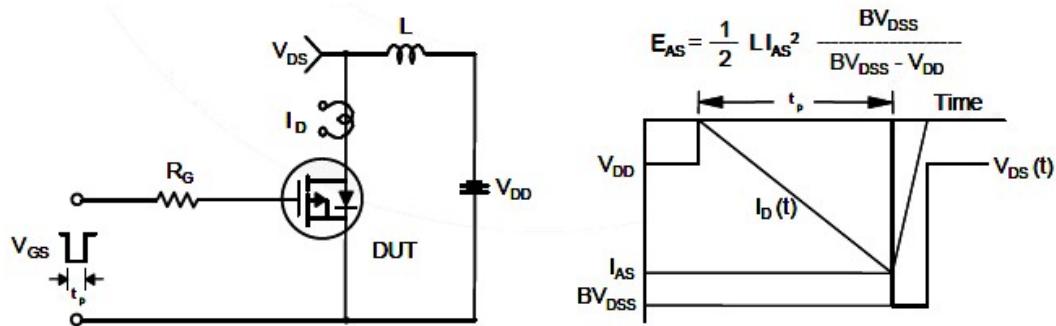
Note:

- ① Repetitive rating; pulse width limited by max, junction temperature.
- ② Limited by T_j max, starting $T_j=25^\circ\text{C}$, $L=0.1\text{mH}$, $R_G=2\Omega$, $I_{AS}=-5\text{A}$, $V_{GS}=-10\text{V}$, Part not recommended for use above this value
- ③ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$



Test circuit

(1) Unclamped inductive test circuits and waveforms



(2) Switching time test circuit and waveforms

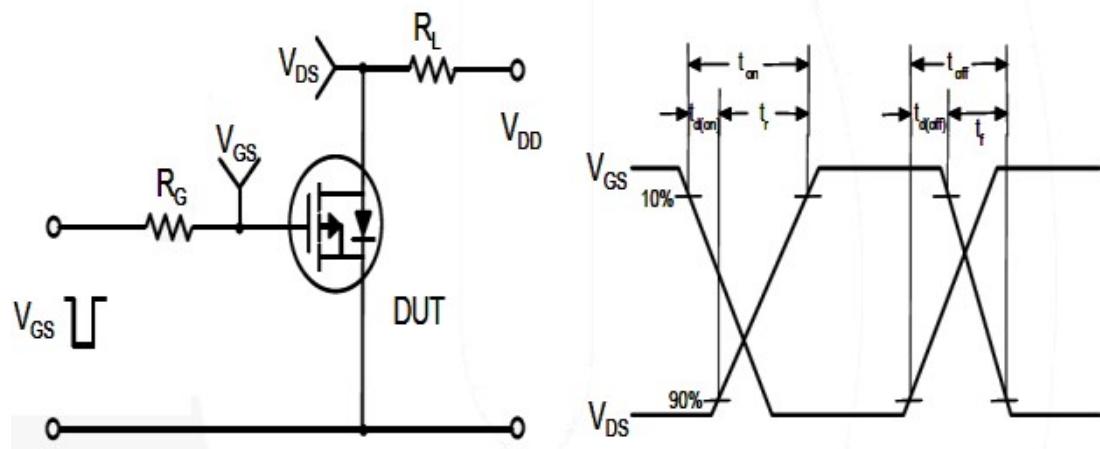




Fig 1. Typical Output Characteristics

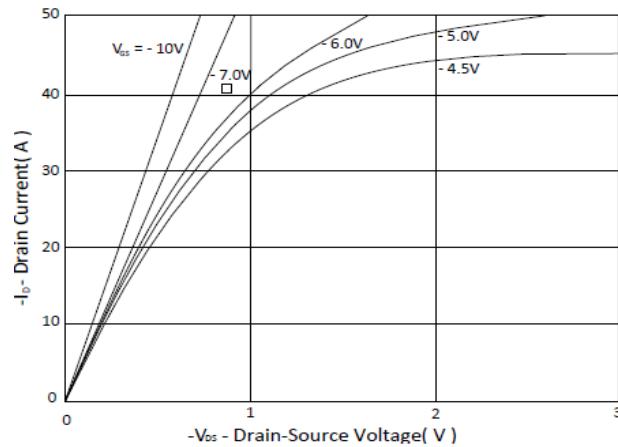


Figure 2. On-Resistance vs. Gate-Source Voltage

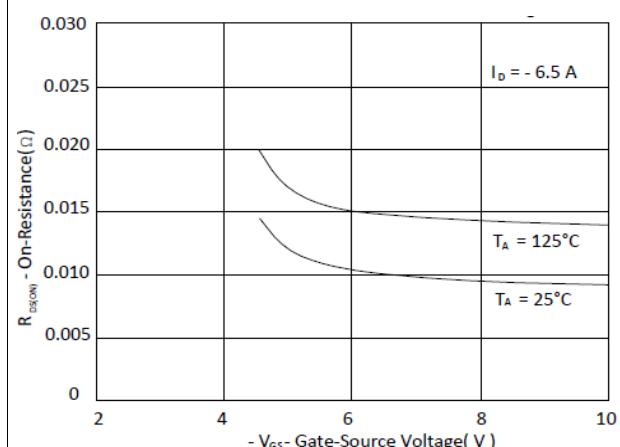


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

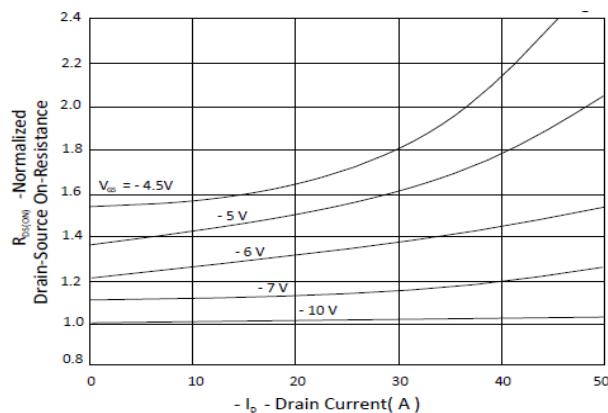


Figure 4. Normalized On-Resistance vs. Junction Temperature

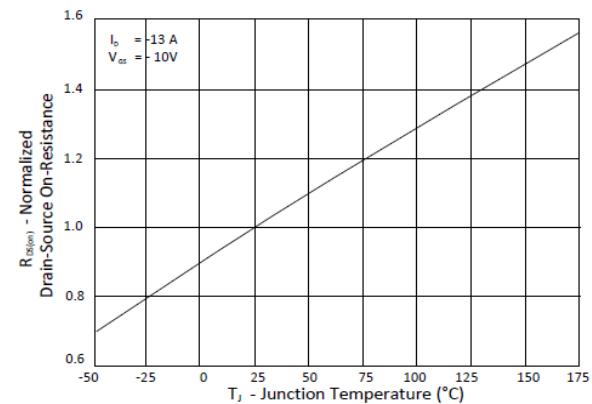


Figure 5. Typical Transfer Characteristics

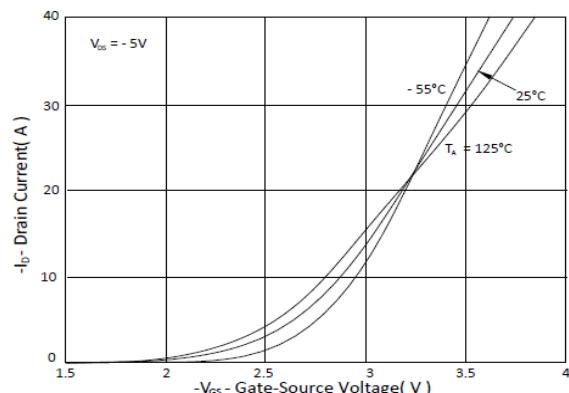


Figure 6. Typical Source-Drain Diode Forward Voltage

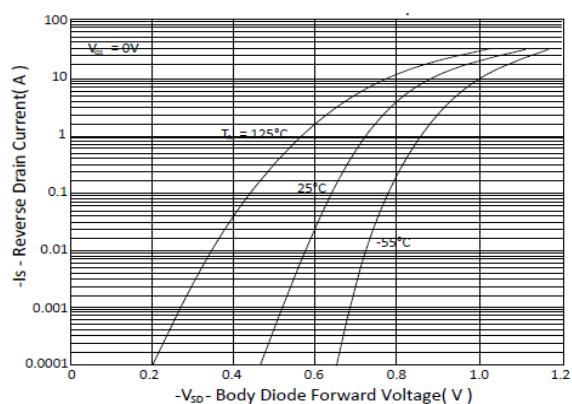




Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

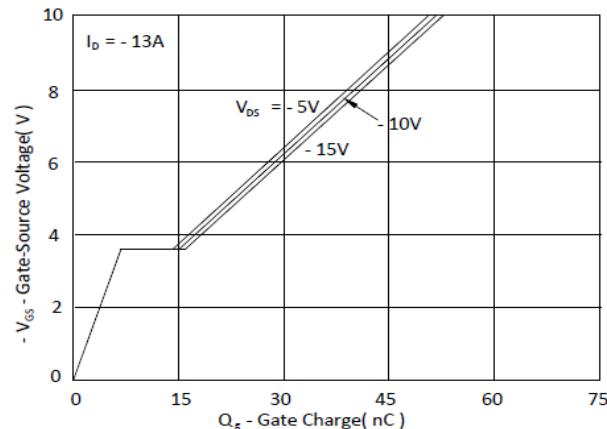


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

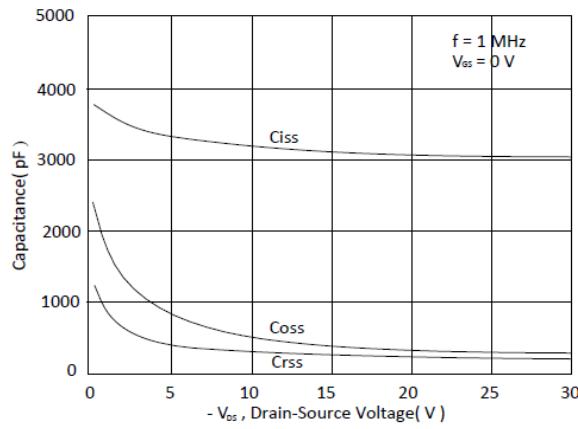


Figure 9. Maximum Safe Operating Area

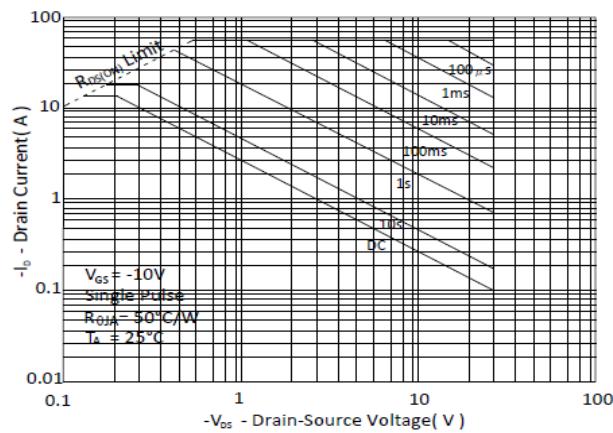


Figure 10. Single Pulse Maximum Power Dissipation

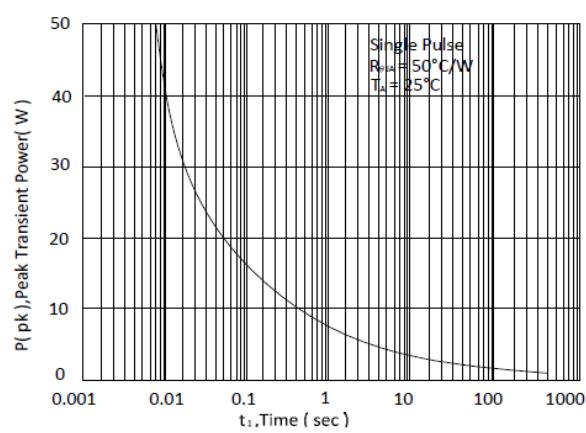
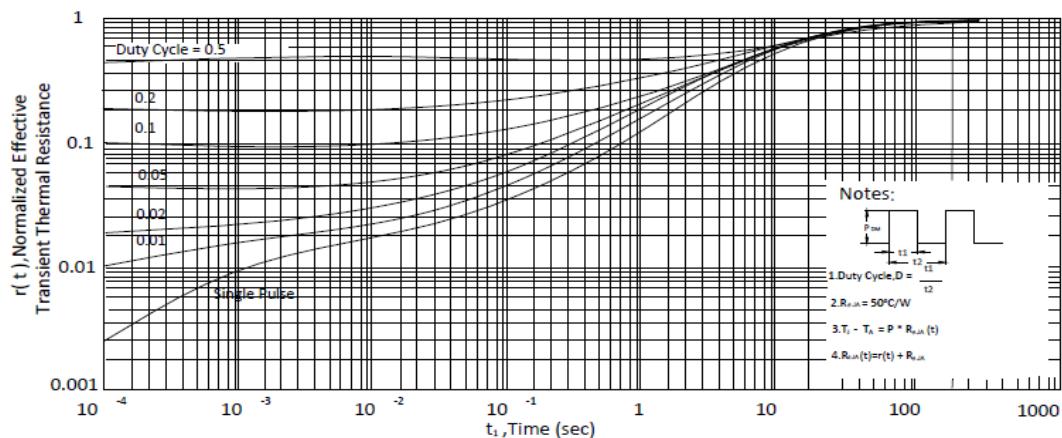
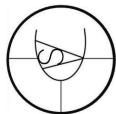


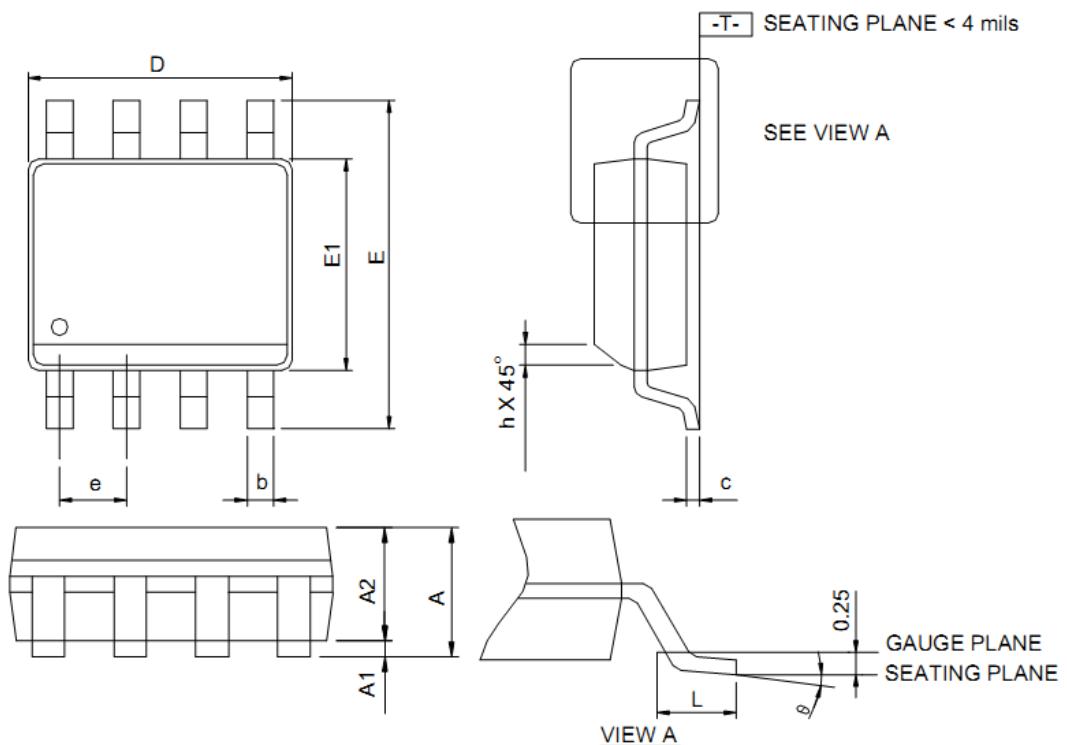
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient





Package Information

SOP-8L



SYMBOL	SOP-8L			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

- Note:
1. Follow JEDEC MS-012 AA.
 2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
 3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

